General Description

The Digital Blocks DB9000AXI5 Display Controller IP Core interfaces a microprocessor and frame buffer memory via an AMBA AXI5 / ACE5-Lite Protocol Interconnect to a TFT LCD or OLED display panel. It is the DB9000AXI4 core with an AXI5-capable read master: coherent, real-time and safety-ready, for SoCs whose interconnect has moved to AMBA 5.

AXI5 is defined as a set of independently negotiable interface properties rather than a single compliance level, and the DB9000AXI5 follows that model. Each property below is an independent synthesis option, licensed and built only where required; with every property disabled the DB9000AXI5 is functionally an AXI4 core, and all AXI5 registers reset such that a reset core behaves exactly as the DB9000AXI4 does today. There is no flag day for existing designs.

Figure 1 depicts the system view of the DB9000AXI5 Display Controller IP Core embedded within an ASIC, ASSP or FPGA device.

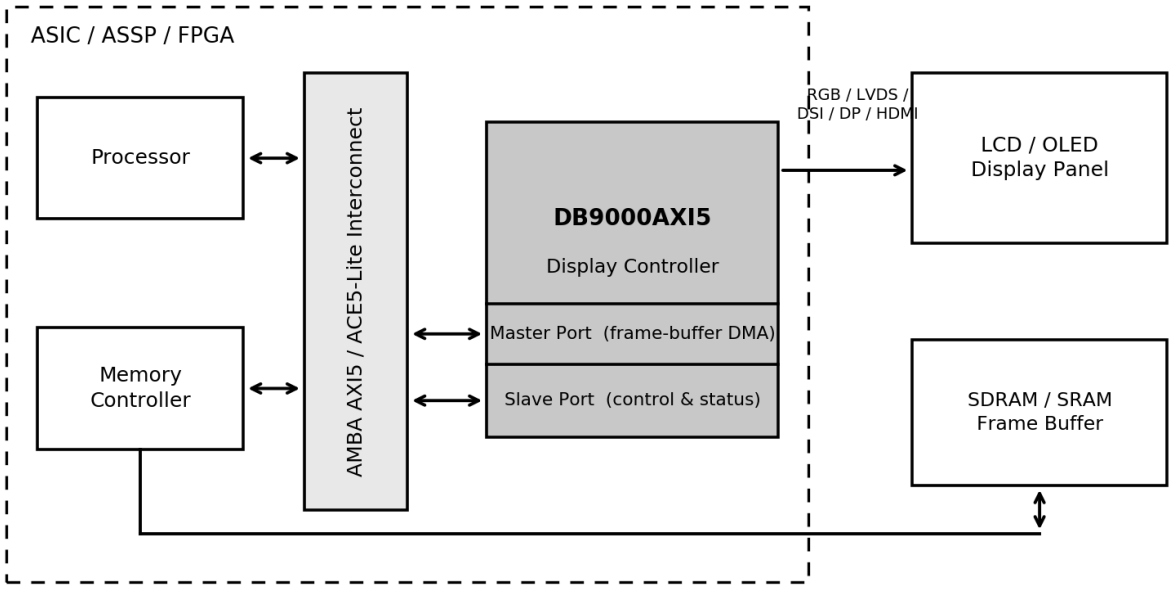

Figure 1: DB9000AXI5 Display Controller System View

AXI5 Features

- ACE5-Lite I/O coherency:
  - The display reads frame buffers through the coherency fabric, snooping CPU and GPU caches, and receives current data whether it is in memory or still dirty in a cache — the cache-maintenance calls in the frame buffer driver are removed and the frame buffer is allocated as normal cacheable memory
  - ReadOnce and ReadOnceMakeInvalid snoop transactions (ARDOMAIN, ARSNOOP); deallocating reads for the base screen, which consumes each line exactly once per frame
  - The controller has no cache of its own, so it is never snooped — no snoop address, response or data channel is added
- Guaranteed bandwidth and latency:
  - MPAM partition identifier per transaction (ARMPAM), allocating the display a guaranteed share of shared-cache capacity and memory bandwidth rather than a priority hint
  - Per-requester QoS (ARQOS) for base screen, overlay windows, cursor and frame descriptor fetches, plus the full AXI4 control set — ARCACHE, ARPROT, ARREGION

  - Read data chunking (ARCHUNKEN, RCHUNKV, RCHUNKNUM, RCHUNKSTRB): long bursts for DRAM page efficiency with early, possibly out-of-order chunk return — shortening time-to-first-pixel at start of frame and start of line, and speeding Input FIFO recovery after a bandwidth excursion. The master falls back to strictly in-order return when the completer does not support chunking
- Functional safety:
  - AXI5 check / parity signal groups across address, ID, control, data, response and handshake, generated on what the core drives and verified on what it receives; each sub-group independently enabled
  - RPOISON handling — data known to be corrupt (for example an uncorrectable DRAM ECC error) is detected before it reaches the panel, rather than being displayed
  - Errors are logged with the failing channel and transaction ID and raise a dedicated bus-check-error interrupt; a programmable safe-state response policy selects the deterministic behavior on a detected poison or check error
  - Complements the CRC Check Per Region and Frozen Display Monitor options to form three layers of display-path integrity checking
- Protected media path:
  - Non-secure Access Identity (ARNSAID) and RME security state (ARNSE) let the controller read TrustZone-protected HDR and DRM video surfaces that the host CPU cannot, and composite them with unprotected graphics planes
- Wakeup, trace and wide data:
  - AWAKEUP signalling so the interconnect and memory system leave low-power states deterministically ahead of a frame rather than being woken by the first transaction
  - ARTRACE / RTRACE transaction tagging for system trace capture, correlating an Input FIFO underrun event with interconnect activity
  - Data width parameterizable to 1024 bits
- Property-selectable: every AXI5 feature above is an independent synthesis option; all disabled equals DB9000AXI4

Display Controller Features

- Wide range of programmable display panel resolutions:
  - 8K / 4K / HD high-resolution displays down to 320×240 panels; maximum programmable resolution 4096×4096 per port
  - Horizontal pixel resolutions from 16 to 4096 pixels in 16-pixel increments
- Programmable 1, 2, 4 or 8-port LCD / OLED display panel interface:
  - 18-bit digital (6 bits/color) and 24-bit digital (8 bits/color) parallel RGB
  - Interfaces to LVDS, MIPI DSI, DisplayPort, DVI, HDMI, V-by-One and BT.656 transmitters
- Programmable frame buffer bits-per-pixel (bpp) color depths:
  - 1, 2, 4, 8 bpp mapped through the Color Palette
  - 16, 18, 24 bpp driving the panel directly (30 bpp with the HDR option)
  - Programmable output format: RGB 6:6:6 / 5:6:5 / 5:5:5 on the 18-bit interface, RGB 8:8:8 on the 24-bit interface
- Color Palette RAM to reduce frame buffer storage and bus bandwidth:
  - 256-entry × 16-bit RAM, implemented as 128 entries × 32 bits
  - Loaded through the Slave Port statically by the microprocessor, or through the Master Port dynamically each frame by the DMA controller
- Programmable horizontal and vertical timing parameters — front porch, back porch, sync width, pixels-per-line, lines-per-panel, and sync polarity
- Programmable pixel clock — divider from 1 to 128 of the bus clock, programmable polarity, or direct drive from an external pixel clock
- Programmable Data Enable timing signal, derived from the horizontal and vertical timing parameters, with programmable polarity
- AMBA AXI5 interconnect:
  - Selectable 1024 / 512 / 256 / 128 / 64 / 32-bit AXI5 Master Port for DMA access of frame buffer memory
  - Selectable AXI4-Lite (or AHB / APB) Slave Port for the control & status interface to the microprocessor
  - Programmable outstanding read requests and burst lengths up to 256 beats
  - 64-bit frame buffer addressing through the address-extension register
- Three memories:

  - Input FIFO decoupling the bus clock from the panel pixel clock, integrated with the DMA controller
  - 256-word × 16-bit Color Palette RAM
  - Output FIFO
  - FIFOs parameterizable in depth and width
- Linux OS frame buffer driver supplied with the core; with I/O coherency enabled the driver's cache-maintenance path is removed
- Power up and down sequencing support, with PWM backlight control
- 15 (plus the AXI5 bus-check-error interrupt) sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- Compliance with the following specifications:
  - AMBA AXI Protocol Specification — AXI5 and ACE5-Lite
  - AMBA AXI4-Lite / AHB / APB for the control & status Slave Port
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks and no internal tri-states

Display Resolution Support — Additional Information

Example high resolutions: Digital Cinema Systems (DCI) 2048×1080 2K and 4096×2160 4K images, and Cinema Scope HD 2560×1080.

Example high resolutions: 7680×4320, 4096×2560, 3840×2160, 2560×2048, 2048×2048, 2048×1536, 1920×1200, 1920×1080, 1680×1050, 1600×1200, 1600×900, 1440×900, 1366×768, 1280×1024, 1280×768, 1080×1920, 1024×768, 1024×600, 1024×576, 960×540, 800×600, 800×480.

Example medium / small resolutions: 640×480, 640×400, 640×240, 640×200, 480×800, 480×640, 480×272, 480×234, 320×240, 320×200, 240×400, 240×320, 240×240.

Display Controller — Block Diagram

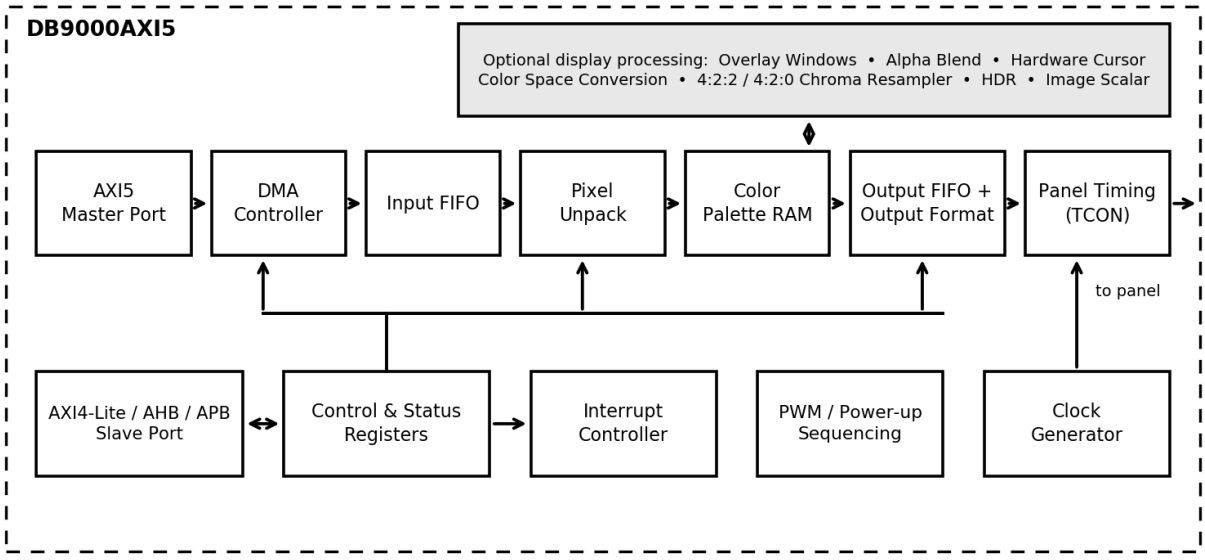

Figure 2: DB9000AXI5 Display Controller Block Diagram

Configuration Options

Every DB9000 shipment is a synthesizable Verilog RTL core, not a fixed netlist. Bus protocol, bus width, memory technology and FIFO sizing are all set by `define / parameter before synthesis, and each advanced feature is only built into the gate count if it is licensed and enabled — so an unlicensed feature costs zero silicon.

Core Synthesis Parameters — available in every DB9000 configuration, no licensing required.

Parameter	Description
Bus Protocol & Interconnect	AMBA AXI5 / ACE5-Lite, AXI4, AXI3, AHB5, AHB, AHB-Lite, APB, or Altera

	Avalon-MM — selected by a single Verilog `define.
Master Bus Data Width	32-, 64-, 128-, 256- or 512-bit master bus, sized to the target resolution and bandwidth.
Memory Technology Target	Palette, FIFO and Cursor memories instantiate through one wrapper module, pre-built for Xilinx, Altera, Actel or a generic vendor RAM — or substitute your own.
Synchronous / Asynchronous FIFOs	Input / Output FIFOs default to synchronous; a single `define switches to asynchronous, unregistered-output memories.
Configurable FIFO Depth	Input FIFO address width sets FIFO depth — typically 16 words for small panels, up to 2K words for large, high-resolution panels, with data width scaling to the master bus.
Pixel Clock Source Select	Internal clock-mux architecture with full CR1 programming, or a direct bypass `define that drives the pixel clock straight from PCLK_IN.
Register Bit Trimming	Any unused Control & Status Register bit can be removed and hardwired as a parameter instead — typically halving VLSI footprint versus a fully-populated register set.
DFT Test Bus Passthrough	Optional per-memory DFT test buses netlist up to the top level for scan / BIST insertion.

Licensing & Synthesis Options — optional RTL add-ons, each independently licensable and synthesized only when enabled.

Option	Description
Multi-Window Compositing	
Overlay Windows	1, 2, 4, 8 or 16 independently positioned, DMA-fed overlay windows composited over the base screen, each with its own enable, X/Y start-end and frame-buffer address registers.
Alpha Blend	Per-pixel alpha compositing of an Overlay Window over the base screen at 16 / 18 / 24 bpp, with an 8-bit alpha channel and programmable alpha inversion.
Hardware Cursor	32×32 or 64×64 pixel hardware cursor with its own palette, X/Y positioning and clip registers, sourced from a dedicated dual-port cursor buffer memory — zero host involvement per frame.
Image Scalar (Preliminary)	In-line image scalar within the display controller for ASICs — scaling is applied directly to the pixel stream before it reaches the display interface, with independent scaling per plane.
Color Space & Chroma Processing	
Chroma Resampler — 4:2:2 / 4:2:0	Up-samples packed YCbCr 4:2:2 (2-tap FIR) or planar 4:2:0 video (parallel-DMA, cubic-convolution engine) to 4:4:4 ahead of color-space conversion.
Color Space Conversion	Programmable 4×4 matrix (10-bit signed coefficients, 8-bit summands) converts YCbCr to gamma-corrected RGB, with selectable truncate / round and saturate / clamp behavior; up to three instances — base screen plus two overlay windows.
High Dynamic Range (HDR) (Preliminary)	HDR10 / HLG pixel path: 30 bpp (10:10:10) frame buffers, 10-bit output dithered to 8-bit panels, programmable PQ / HLG / BT.1886 LUTs, a BT.709 ↔ DCI-P3 ↔ BT.2020 gamut matrix in linear light, and BT.2390 tone mapping. ST 2086 metadata sideband. Optional 3D LUT and per-plane HDR.
Advanced Panel Interfaces	
LVDS Serializer (OpenLDI)	OpenLDI V0.95-compliant serializer driven by a customer-supplied 7× pixel clock, generating 18- or 24-bit RGB LVDS output pairs plus VSYNC / HSYNC / DE — Unbalanced mode standard, Balanced mode by request.
Multi-Port / Multi-Link Interface + UHD Output Formatter	1, 2, 4 or 8-lane output to DisplayPort, HDMI, V-by-One, MIPI or LVDS panels, with single / dual / quadrant screen-area partitioning for UHD / 8K displays. Supersedes the earlier fixed 2-port interface as of Release 1.15.0.
Dual Display Support	Splits one unified frame buffer line in half in hardware to drive independent left / right displays from a single pixel pipeline running at 2× pixel clock.
Dynamic Content Engine	
Frame Descriptor Engine	Linked-list DMA engine that reprograms the base-screen and up to 16 overlay-window frame-buffer addresses before every frame with zero host CPU intervention — built for streaming video playout.
Diagnostics & Reliability	
Test Pattern Generation (Preliminary)	On-demand RGB color bars, grayscale gradient or border-grid test patterns triggered by a register write — no external stimulus required.
CRC Check Per Region (Preliminary)	Hardware CRC-802.3 checking of incoming frame-buffer pixel data across 32-, 64-, 128-, 256- or 512-bit bus widths, with programmable per-region checking and automatic retransmission or interrupt on error.
Frozen Display Monitor (Preliminary)	Watchdog-timed monitor of VSYNC / HSYNC / DE and the DMA base-to-current-address heartbeat, with optional automatic self-reset and re-run on a detected

	fault.

Items marked Preliminary are specified but not yet released; contact Digital Blocks for status. Full register-level detail for every option is documented in the DB9000 Technical Reference Manual.

Pin Description

In addition to the AMBA AXI5 / ACE5-Lite Master and AXI4-Lite / AHB / APB Slave Bus interfaces, which include the input clock and reset signals and the output INTR (interrupt) signal, the interface to the display panel is listed in Table 1. The AXI5 property signals listed above are present only when the corresponding synthesis option is enabled. Note that if the panel is 18-bit data, the lower 6 bits of LCD_R, LCD_G and LCD_B should be connected. In multi-port and multi-link configurations the panel interface is replicated per port.

Name	Type	Description
LCD / OLED Panel Interface		
LCD_PCLK	Output	Pixel Clock
LCD_HSYNC	Output	Horizontal Sync Pulse
LCD_VSYNC	Output	Vertical Sync Pulse
LCD_DE	Output	Display Enable
LCD_PE	Output	Power Enable
LCD_R[7:0]	Output	Red Data
LCD_G[7:0]	Output	Green Data
LCD_B[7:0]	Output	Blue Data

Table 1: DB9000AXI5 — I/O Pin Description for Interface to the Display Panel

Verification Method

The DB9000AXI5 is verified with an AXI5 bus functional model that programs the control & status registers via the Slave Bus, returns frame buffer data in response to Master read requests, and checks expected results. For the AXI5 properties the model adds configurable response latency and bandwidth throttling, chunked read return with programmable chunk ordering, poison and check-signal error injection, and a coherency model whose writes are visible only through snooping — so a missing or incorrect snoop request fails in simulation rather than on silicon.

The underlying DB9000 display pipeline is silicon-proven and FPGA-proven driving TFT LCD and OLED panels from 320×240 up to 4K and 8K resolutions.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AXI5. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AXI5 is available in synthesizable RTL Verilog, along with a simulation test suite, Linux driver, Synopsys Design Constraints (SDC), a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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