General Description

The Digital Blocks DB9100AHB BitBLT Graphics Hardware Accelerator Verilog IP Core renders a graphics frame by generating new bitmaps from commands to combining existing bitmaps on and off-screen using one of 256 Raster Operations. A Raster Operation (ROP) is a bitwise Boolean operation (such as AND, OR, XOR, NOT).

The DB9100AHB also contains a Monochrome Bitmap Color Expansion feature, typically used for font expansion of compressed character bitmaps. A 1-bit depth bitmap is expanded to one of two colors, a foreground or background color, with the foreground color representing the text, and the background color the non-text background.

The DB9100AHB also contains a programmable Alpha Blend unit, blending two bitmaps into one.

The DB9100AHB interfaces to a microprocessor and frame buffer memory via the AMBA AHB Interconnect, providing high performance memory throughput. The DB9100AHB contains a DMA Command Linked-List Processing Unit, for independently reading and processing graphics commands from the host processor.

Figure 1 depicts the system view of the DB9100AHB BitBLT Graphics Hardware Accelerator Verilog IP Core embedded within an ASIC, ASSP, or FPGA component.
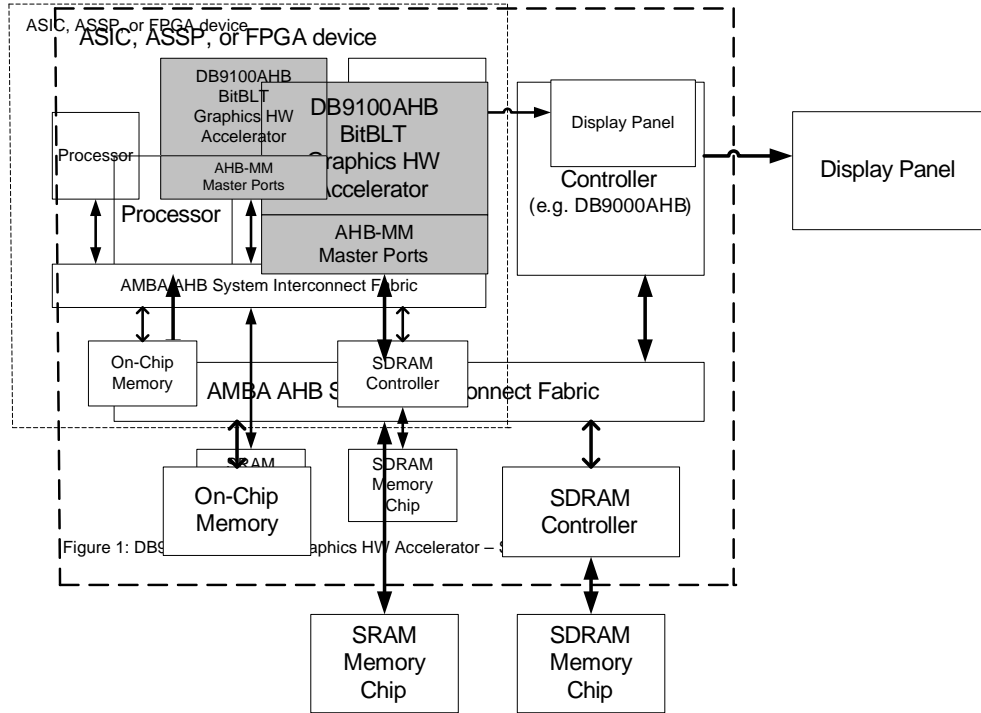
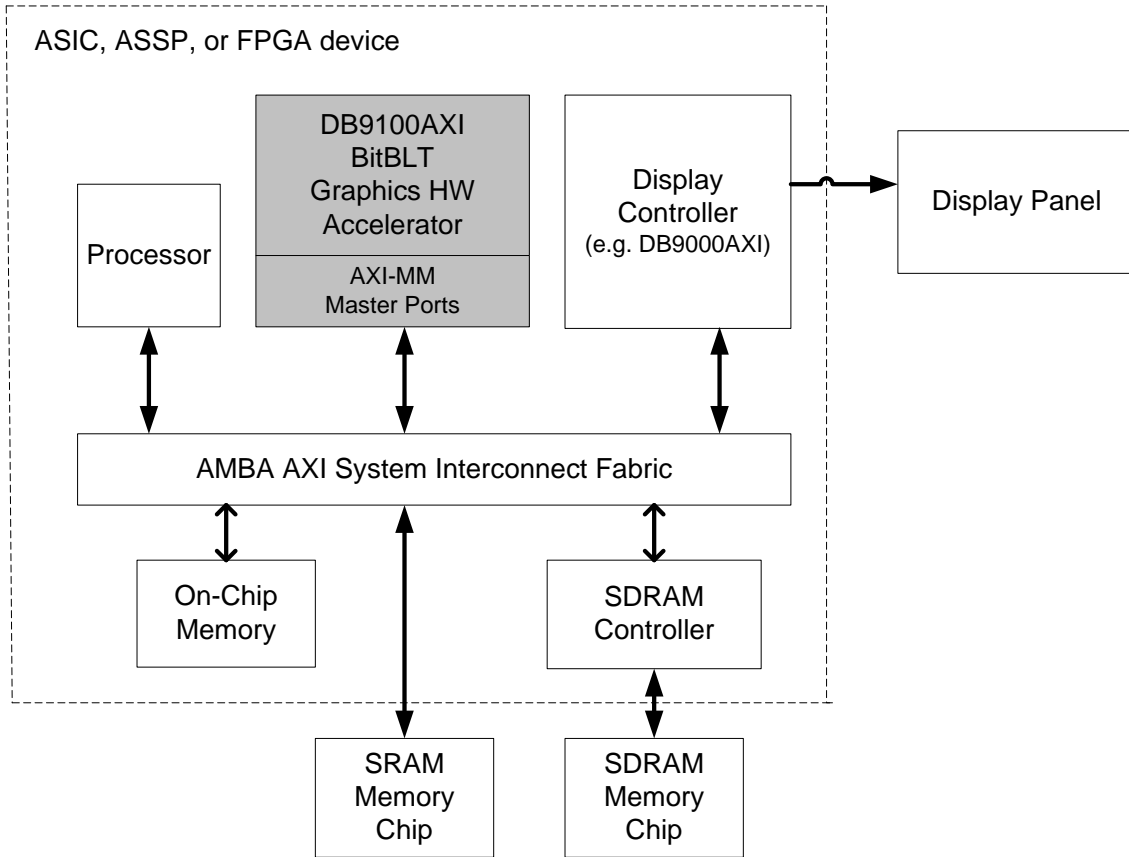Figure 1: DB9100 AHB BitBLT Graphics HW Accelerator – System Diagram

Figure 1: DB9100AXI BitBLT Graphics HW Accelerator – System Diagram

BitBLT Graphics Hardware Accelerator Verilog IP Features

- Bit Block Transfer – 3 Independent Memory Sources of data:
    - On-Screen & Off-Screen Data Block (SRC)
    - Off-Screen Fixed Pattern Data Block (PTN)
    - On-Screen visible Data Block (DST)
- Raster Operations (ROP) performed on Block Transfers:
    - 256 Raster Operations
    - ROP0, ROP1, ROP2, & ROP3 operations
    - Includes industries most popular 16 ROPs
- BitBLT Draw Features:
    - Pixels, Horizontal & Vertical Lines
    - Overlapping & Non-Overlapping Block Transfers
    - Solid Color Block Fills
    - FONT Monochrome Bitmap to Color Expansion, either Transparent or Opaque
    - Rotation Block Transfers: 0, 90, 180, 270 degrees
    - Block Stretch on X & Y Axis
    - Alpha Blending
    - Sprite Moves
- Command FIFO or Link-List Display Processing Unit:
    - Simplifies Processor Interface
    - Minimizes Processor Overhead
- Frame Buffer & Display Features Supported:
    - Display Resolutions 4K x 4K
    - 4 GB Memory Range
    - 8, 16 , 24, & 32 bits-per-pixel color depths
- Interrupt Controller with 3 sources of internal interrupts with masking control
- Reference Software Driver Included
    - Reference Driver
    - Graphics API Reference Design
- On-Chip Interconnect Compliance - AHB:
    - AMBA AHB Specification 2.0
- FPGA Integration Support:
    - Altera Quartus II & Qsys Integration & ARM / NIOS II EDS Reference Design
    - Xilinx Vivado IP Integrator & Reference Design

- ASIC / ASSP Design-In Support:
    - Compliance to RTL Design, Coding, & Verification Standards
    - Digital Blocks Support Services
- Compatible with Digital Blocks DB9000 Family of TFT LCD Controller IP Cores and Reference Designs
- Fully-synchronous, synthesizable Verilog RTL core.

Deliverables

The DB9100AHB is available in RTL Verilog, along with synthesis scripts, a simulation test bench with expected results, reference design, datasheet, and user manual.

Support

The DB9100AHB IP Core is warranted against defects for three years. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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