Digital Blocks Validates Existing I2C Slave Controller IP Core Family Compatibility with MIPI I3Cs

GLEN ROCK, New Jersey, Nov 6, 2016 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals requirements, extends its leadership in I2C Controller Verilog IP Cores with validation of its existing I2C Slave Controller family with the emerging MIPI I3C (Improved Inter Integrated Circuit) standard.

Digital Block I2C Slave Controller Verilog IP Cores, in addition to operating withing a NXP I2C bus, can integrate into an I3C bus and communicate with a MIPI I3C Master. Digital Block I2C Slave IPs compatible with the MIPI I3C standard are the following:

DB-I2C IP Core	Product Description
DB-I2C-S-AVLN	I2C Controller IP - Slave, Parameterized FIFO, AVLN Bus
DB-I2C-S-APB	I2C Controller IP - Slave, Parameterized FIFO, APB Bus
DB-I2C-S-AHB	I2C Controller IP - Slave, Parameterized FIFO, AHB Bus
DB-I2C-S-AXI	I2C Controller IP - Slave, Parameterized FIFO, AXI Bus
DB-I2C-S-SCL-CLK	I2C Controller IP - Slave, SCL Clock only, principally for configuring registers in mixed-signal ICs with low noise or low power requirements
DB-I2C-S-SCL-CLK-APB	I2C Controller IP - Slave, SCL Clock, Parameterized FIFO, APB Bus. For low power requirements in I2C Slave Controller interface to CPU.

Price and Availability
The DB-I2C Core Family have led the industry since 2006 and are available in synthesizable Verilog RTL, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at http://www.digitalblocks.com and http://www.digitalblocks.com/I2C-IP-Core-Reference-Design.html

About Digital Blocks
Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with requirements for Embedded Processor & Peripherals, TFT LCD Display Controllers & Processors, 2D Graphics Hardware Accelerator Engines, LVDS Display Link Layer Drivers, Video Signal & Image Processing, and Low-Latency TCP/UDP/RTP Hardware Protocol Stacks for High-Speed Networking.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks

is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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