Digital Blocks I2C & SPI Controller IP Core Families Extend Leadership in Sensor Interface to Host Processors with System-Level Features & Low Power

GLEN ROCK, New Jersey, April 13, 2016 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals requirements, extends its leadership in I2C and SPI Controller Verilog IP Cores targeting IC Sensor interfaces to Host Processors.

Digital Block separate I2C and SPI Controllers target both the Host Processor and the Sensor IC Interface to the I2C and SPI Buses. Digital Blocks Verification suite targets the following Sensor IC Applications:

- Accelerometers / Gyroscopes / Compass / Magnetometers
- Humidity, Gas/Chemical, Pressure, Temperature, UV Index, Ambient Light
- Capacitive Touch
- Proximity
- Digital Color
- Automotive, Medical, IoT, Wearables, SmartPhones

I2C and SPI Verilog IP Core Common Features are the following:

- Master/Slave, Master-only, & Slave-only I2C or SPI Controller Verilog IP
- Finite State Machine control unit to off-load the I2C or SPI transfer from the Processor
- TX, RX, TX/RX FIFO configuration options, dual clock design, parameterized depth
- CPU Interface via APB/AHB/AHB-lite/AXI4/AXI4-lite/AXI3/Avalon bus fabrics
- Similar Programming Architectures
- Low Power Design

Inter-Integrated Circuit (I2C) Controller Verilog IP Core Features are the following:

- Full range of I2C Bus Speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s), Fast mode plus (1 Mbit/s), Ultra-Fast-mode (5 Mbit/s) & Hs mode (3.4+ Mb/s)
- Multi-Master, Arbitration, Clock Synchronization (Master Features)
- SCL Pulled Low Wait States
- Enhanced SCL / SDA spike filtering capabilities
- SMBus Compatible (optional)
- HID over I2C (optional)

Serial Peripheral Interface (SPI) Controller Verilog IP Core Features are the following:

- SPI Bus Speeds programmable up to 200 Mbit/s
- Static SPI clock design for lowest power
- 4 and 3 wire SPI Interfaces
- Quad/Dual/Single Data Lanes

Price and Availability
The DB-I2C and DB-SPI IP Core Family are available immediately in synthesizable Verilog RTL, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at http://www.digitalblocks.com

About Digital Blocks
Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with requirements for Embedded Processor & Peripherals, TFT LCD Display Controllers & Processors, 2D Graphics Hardware Accelerator Engines, LVDS Display Link Layer Drivers, Video Signal & Image Processing, and Low-Latency TCP/UDP/RTP Hardware Protocol Stacks for High-Speed Networking.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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