Digital Blocks Extends its MIPI I3C Controller IP Core Family with I3C Master/Slave, I3C Master, and I3C Slave Releases.

The DB-I3C IP Core Family offers a comprehensive solution to Sensor connection to Host CPUs.

GLEN ROCK, New Jersey, July 29, 2018 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals requirements, extends its leadership in MIPI I3C Controller Verilog IP Cores targeting IC Sensor interfaces to Host Processors.

The MIPI I3C Controller family include the following:

The **DB-I3C-M** Controller IP (I3C Master only) interfaces an on-chip Host Controller processor via AMBA APB, AHB, or AXI-Lite to external sensor MIPI I3C Slaves.

The **DB-I3C-S** Controller IP (I3C Slave only) interfaces an embedded processor via on-chip AMBA APB, AHB, or AXI-Lite interconnect to external MIPI I3C Master.

The **DB-I3C-S-REG** Controller IP (I3C Slave only) interfaces a sensor's registers to an external MIPI I3C Master.

The **DB-I3C-MS** Controller IP (I3C Master and Slave) interfaces an embedded processor to the MIPI I3C as either Master or Slave.

Please start with Digital Blocks MIPI *I3C Controller IP Core Reference Design* page for more information https://www.digitalblocks.com/mipi-i3c-ip.html

Price and Availability
The DB-I3C IP Core Family is available immediately in synthesizable Verilog, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at http://www.digitalblocks.com

About Digital Blocks
Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers requiring best-in-class IP for Embedded Processors, I2C/SPI/DMA Peripherals, MIPI I3C peripheral, TFT LCD/OLED Display Controllers & Processors, 2D Graphics Hardware Accelerator Engines, Display Link Layer Drivers, Video Signal & Image Processing, and Low-Latency TCP/UDP/RTP Hardware Protocol Stacks.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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