Digital Blocks DB9000 Display Controller & Processor IP Core Family Extends Leadership Across Medical, Industrial, Aerospace, Automotive, Communications, Computer, Monitor, Consumer, IoT, AR/VR Headsets, Wearables, Signage, and Cinema Applications

GLEN ROCK, New Jersey, April 22, 2019 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with display controller, 2D graphics, or video processing requirements, extends the leadership of the DB9000 Display Controller & Processor IP Core Family across a wide range of applications.

The DB9000 Display Controller & Processor IP is offered with a customer-specific range of features, supporting basic display applications. Advanced releases add optional features, such as support for multiple graphics or video layers, composition, compressed frame buffer, and high dynamic range (HDR).

The DB9000 Display Controller & Processor IP Core supports LCD and OLED panel resolutions from 240x240 up to 8192x8192, with 1,2,4,8,16,18,24,30,32, and 36-bit bits-per-pixel, both RGB and YCrCb color spaces, with interfaces to 1, 2, 4, & 8 port LVDS, MIPI DSI, DVI, HDMI, V-by-One, and DisplayPort.

The DB9000 IP Core supports SoC fabrics interfacing to DDRn DRAM frame buffer memory with memory controller 32-, 64-, 128-, or 256-bit data widths, supporting AXI4, AXI3, AHB, AHB-Lite and Avalon protocols. With respect to the AXI protocol, the DB9000 supports multiple outstanding memory requests, supporting higher resolution panels.

Support for high resolution LCD and OLED panels includes Full High Definition (FHD), Ultra HD (UHD/Quad FHD), Digital Cinema Systems (DCI) 2K & 4K images, and 5K 5120x2880. A representative listing follows:

Format	Resolution
Square	240 x 240
QVGA	240 x 320
	240 x 400
	320 x 240
16:9 Aspect Ratio	480 x 234
	480 x 272
VGA	480 x 640
	640 x 480
WVGA	480 x 800
	800 x 480
SVGA	800 x 600
960x540	960 x 540
WSVGA	1024 x 576
	1024 x 600

Format	Resolution
XGA	1024 x768
SXGA	1280 x 1024
HD / WXGA	1366 x 768
WXGA+	1440 x 900
HD+	1600 x 900
UXGA	1600 x 1200
WSXGA+	1680 x 1050
Full HD	1920 x 1080
	1080 x 1920
WUXGA	1920 x 1200
DCI 2K	2048 x 1080
3M pixels	2048 x 1536
Super Retina HD	2436 x 1125
QHD	2560 x 1440
CSHD	2560 x 1080
5M pixels	2560 x 2048
	2960 x 1440
QFHD / UHD	3840 x 2160
DCI 4K	4096 x 2160
10M pixels	4096 x 2560
14.7M pixels	5120 x 2880

Price and Availability
The DB9000 Display Controller & Processor IP Core family is available in synthesizable Verilog, along with a comprehensive simulation test suite, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at http://www.digitalblocks.com/ip-cores/tft-lcd-display-controller-verilog-ip-core.html

About Digital Blocks
Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers requiring best-in-class IP for Embedded Processors, I2C/SPI/DMA Peripherals, TFT LCD/OLED Display Controllers & Processors, 2D Graphics Hardware Accelerator Engines, LVDS Display Link Layer Drivers, Video Signal & Image Processing, and Low-Latency TCP/UDP/RTP Hardware Protocol Stacks.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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