

## **Digital Blocks Announces its “Try Before You Buy” IP Core Evaluation Program**

*Prospective customers can evaluate Digital Blocks VHDL / Verilog IP cores prior to licensing, in a variety of formats.*

**GLEN ROCK, New Jersey, April 24, 2006** – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor system designers, today announces the “Try Before You Buy” IP Core Evaluation Program for all product offerings. Prospective customers have one-of-three options to evaluate a Digital Blocks IP Core: (1) Modelsim compiled simulation-only model with testbench; (2) Time-limited hardware model programmed into an FPGA; and (3) Altera OpenCore Model for evaluation within Quartus II or Altera FPGAs.

Currently, prospective customers can evaluate Digital Blocks’ DB8259A Programmable Interrupt Controller, which maintains the original static design of the Intel 8259A and Harris / Intersil 82C59A devices, the DB8259S Programmable Interrupt Controller, which adds a clock for an all synchronous design, and the DB6845 CRT Controller.

For time-limited hardware model evaluation, Digital Blocks supports Actel, Altera, Lattice, Quicklogic, and Xilinx, FPGAs.

Customers interested in evaluating Digital Blocks’ IP should fill out the IP Core Evaluation Request form at Digital Blocks’ web site, [www.digitalblocks.com](http://www.digitalblocks.com).

### **About Digital Blocks**

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer’s development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: 1-201-251-1281; Fax: 1-208-379-1012; Media Contact: [info@digitalblocks.com](mailto:info@digitalblocks.com); Sales Inquiries: [info@digitalblock.com](mailto:info@digitalblock.com); On the Web at [www.digitalblocks.com](http://www.digitalblocks.com)

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