

Digital Blocks Announces the DB9000AVLN TFT LCD Controller IP Core

Specifically targeted for TFT LCD panels and the Altera NIOS II Avalon Bus, the DB9000AVLN is an out-of-the-box soft IP Core for display system designers.

GLEN ROCK, New Jersey, January 31, 2007 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor and video system designers, today announces the DB9000AVLN TFT LCD Controller IP Core. The DB9000AVLN IP Core targets Altera NIOS II embedded processors with the Avalon Bus requiring TFT LCD panel system requirements.

The DB9000AVLN IP Core specifically and cost-effectively targets TFT LCD panels with 1 Port of 18-bit digital (6-bits/color) or 24-bit digital (8-bits/color) interface. This includes single LVDS/TMDS ports with appropriate external drivers.

The DB9000AVLN IP Core contains programmable features comparable to entry-level ASSP LCD controller chips, including a color palette to reduce frame buffer space and Avalon bus bandwidth. With the cores wide range of programming parameters, the controller can support a wide range of LCD panel resolutions. Representative examples are as follows:

Format	Resolution
Square	240x240
QVGA	320x240
	240x320
16:9 Aspect Ratio	480x272
VGA	640x480
SVGA	800x600
XGA	1024x768
SXGA	1280x1024

Price and Availability

The DB9000AVLN is available immediately in synthesizable Verilog, along with synthesis scripts, a simulation test bench with expected results, reference design, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at <http://www.digitalblocks.com>

About Digital Blocks

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals.

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