Digital Blocks Extends the DB9000 TFT LCD Controller IP Core Family with the availability of the DB9000OCP for the Open Core Protocol 2.2 Interconnect

Specifically targeted for TFT LCD panels and the Open Core Protocol 2.2 On-Chip Interconnect, the DB9000OCP is an out-of-the-box synthesizable soft IP Core for ASIC and ASSP design teams with display system requirements.

GLEN ROCK, New Jersey, August 31, 2007 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor and video system designers, today announces the DB9000OCP TFT LCD Controller IP Core. The DB9000OCP IP Core targets systems-on-chip (SoC) ASSP and ASIC designs containing embedded processors and the Open Core Protocol 2.2 On-Chip Interconnect interfacing SRAM or SDRAM frame buffer memory to a TFT LCD panel.

The DB9000OCP IP Core specifically and cost-effectively targets TFT LCD panels with 1 Port of 18-bit digital (6-bits/color) or 24-bit digital (8-bits/color) interface. This includes single LVDS/TMDS ports with appropriate external drivers.

The DB9000OCP IP Core contains programmable features comparable to entry-level ASSP LCD controller chips, including a color palette to reduce frame buffer space and OCP Interconnect bandwidth. With the cores wide range of programming parameters, the controller can support a wide range of LCD panel resolutions. Representative examples are as follows:

Format	Resolution
Square	240x240
QVGA	320x240, 240x320
16:9 Aspect Ratio	480x272
VGA	640x480
SVGA	800x600
XGA	1024x768
SXGA	1280x1024
UXGA	1600x1200
WUXGA	1920x1200

DB9000 Family of TFT LCD Controllers
The DB9000 family of TFT LCD Controllers supports a variety of bus interfaces to frame buffer memory and processors. Please consult Digital Blocks web site for a complete listing.

Price and Availability
The DB9000OCP is available immediately in synthesizable Verilog or VHDL, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at http://www.digitalblocks.com

About Digital Blocks
Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and risks and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1-201-632-4809; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com;
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