



Digital Blocks Announces Compact DB8051C Microcontroller IP Core for Complex Algorithm Finite State Machine Implementations

The DB8051C-FSM 8-bit Microcontroller's low VLSI footprint and high performance make it particularly suitable for flexible Complex FSM Design

GLEN ROCK, New Jersey, April 27, 2011 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals, Networking, Display Controller, 2D Graphics, and Audio / Video processing requirements, today announces the DB8051C-FSM Microcontroller IP Core for algorithmic complex Finite State Machine (FSM) implementations.

Many times the algorithm complexity of a control application is such that a hard-wired FSM cannot do the job within a reasonable amount of time and with reasonable risk. The DB8051C-FSM 8-bit Microcontroller IP Core, with its low VLSI footprint, 255 MCS@51 Binary Compatible Instructions, and a high number of user selectable I/O, brings high-level programmability to the algorithm development & implementation process.

Price and Availability

The DB8051C-FSM is available immediately in synthesizable Verilog along with synthesis scripts, a simulation test bench with expected results, installation guide, and a technical user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at <http://www.digitalblocks.com>

About Digital Blocks

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA).

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