# Digital Blocks Releases 2nd Gen UDP/IP Hardware Stack / UDP/IP Off-Load Engine (UOE) Targeting High-Frequency Trading Systems

*Digital Blocks showcases its UDP/IP Off-Load Engine by appointment at the Low Latency Summit at Convene Conference Center, 730 3rd Avenue, New York, NY*

**New York, Nov 12, 2013** – Digital Blocks, a leading developer of ultra-low latency networking IP Cores for FPGA accelerated Financial Applications on High-Frequency Trading Systems, today releases 2nd Gen DB-UDP-IP-HFT IP Core, a UDP/IP Hardware Stack / UDP Off-Load Engine (UOE) targeting Altera Stratix V and Xilinx Virtex 7 FPGAs on leading-edge network adapter cards with one or more 10 / 40 GbE network links.

Digital Blocks' UDP/IP Off-Load Engine (UOE) targets trading systems with sub-microsecond packet transfers between Network wire and Host. Embedded is a high-performance Direct Memory Access Controller (DMAC) for low-latency, parallel packet payload transfers between memory and Digital Blocks UP/IP packet engines.

*Along with FPGA design services, Digital Blocks works with Financial Trading companies in architecture & design of proprietary trading systems*. Please go to Digital Blocks HFT page for more information www.digitalblocks.com/High-Frequency-Trading-IP-Cores-And-Systems.html as well as Digital Blocks brief data sheet on the UDP Off-Load Engine http://www.digitalblocks.com/files/DB-UDP-IP-HFT-DS-V1-1.pdf

**Price and Availability**
The DB-UDP-IP-HFT IP Core is available immediately in synthesizable Verilog, along with a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at http://www.digitalblocks.com

**About Digital Blocks**
Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with High-Frequency Trading Networking, High-Speed Networking, Networking of Audio/Video, and Display Link Layer IP.

Digital Blocks also serves the Embedded Processor & Peripherals, Display Controller, 2D Graphics, and Audio / Video processing IP Core requirements of SoC / ASIC / FPGA developers.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; eFax: +1-702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com; Twitter at twitter.com/DigitalBlocksIP

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