Digital Blocks Extends its I2C Controller IP Core Family with More Enhanced Capabilities & System-Level Features

The DB-I2C IP Core Family targets applications with full CPU off-load requirements and deep system-level integration capabilities.

GLEN ROCK, New Jersey, June 17, 2014 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals requirements, announces 2014 extensions to its DB-I2C-MS / DB-I2C-M / DB-I2C-S I2C Controller IP Core family, with the following enhanced system-level features & integration capabilities:

- Full range of I2C Bus Speeds: Standard mode (100 Kb/s), Fast mode (400 Kb/s), Fast mode plus (1 Mbit/s), Ultra-Fast-mode (5 Mbit/s) & Hs mode (3.4+ Mb/s)
- Finite State machine control unit to completely off-load the I2C transfer from the CPU
- CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon interconnect fabrics
- DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
- Direct interface to user Registers within ASIC / ASSP / FPGA, for Master/Slave transfer across the I2C Bus
- Enhanced SCL / SDA spike filtering capabilities
- Enhanced Repeated Start capabilities

The DB-I2C family contains I2C compliant features: Multi-Mastering, Clock Synchronization, Arbitration, SCL held low by Slave, Repeated Start, 7/10-bit addressing, & General Call capabilities as well as 100 Kbs, 400 Kbps, 1 Mbps, 3.4 Mbps, & 5 Mbps I2C bus speeds.

The DB-I2C IP Core Family is offered as follows:

Model Number	Description
DB-I2C-MS-APB	I2C Master / Slave parameterized FIFO for targeted interconnect fabrics
DB-I2C-MS-AHB	
DB-I2C-MS-AXI	
DB-I2C-MS-AXI-Lite	
DB-I2C-MS-AVLN	
DB-I2C-M-APB	I2C Master-only parameterized FIFO for targeted interconnect fabrics. Master-only in VLSI space saving format.
DB-I2C-M-AHB	
DB-I2C-M-AXI	
DB-I2C-M-AXI-Lite	

DB-I2C-M-AVLN	
DB-I2C-S-APB	I2C Slave-only parameterized FIFO for targeted interconnect fabrics. Slave-only in VLSI space saving format.
DB-I2C-S-AHB	
DB-I2C-S-AXI	
DB-I2C-S-AXI-Lite	
DB-I2C-S-AVLN	
DB-I2C-S-RA	I2C Slave-only with Digital Blocks unique interface to user Registers
DB-I2C-S-SCL-CLK	I2C Slave-only with SCL clock only, for configuring registers in mixed-signal ICs with low noise or low power requirements
DB-I2C-MS-Hs-Mode	I2C Master / Slave, Master-only, or Slave-only with parameterized FIFO for I2C Hs-Mode Speed
DB-I2C-M-Hs-Mode	
DB-I2C-S-Hs-Mode	

Please start with Digital Blocks *I2C Controller IP Core Reference Design* page for more information www.digitalblocks.com/I2C-IP-Core-Reference-Design.html

Price and Availability

The DB-I2C IP Core Family is available immediately in synthesizable Verilog, along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at http://www.digitalblocks.com

About Digital Blocks

Digital Blocks is a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with Embedded Processor & Peripherals, Display Controller, Display Link Layer, 2D Graphics, Image Compression, Audio / Video processing, and High-Speed Networking requirements.

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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