Digital Blocks Releases 2nd Generation DB9200 Graphics Engine Verilog IP Core Targeting Hardware Accelerated Graphics Display Applications

The DB9200 2D Graphics Engine IP Core accelerates graphics development for ASIC, ASSP, & FPGA design teams, while off-loading the graphics function from the main Processor and enhancing software developer productivity.

GLEN ROCK, New Jersey, June 6, 2014 – Digital Blocks, a leading developer of Display Controller, 2D Graphics Hardware Engines, Display Link Layer, and Audio/Video processing Intellectually Property (IP) soft cores, today releases an enhanced version of the DB9200 2D Graphics Engine Verilog IP Core for low footprint, high-performance hardware accelerated graphics applications.

The DB9200 2D Graphics Engine renders graphics frames by generating bitmaps from graphics instructions as well as combining existing bitmaps on and off-screen using one of 256 Raster Operations; generates characters from compressed bitmaps using its FONT Bitmap Color Expansion feature; performs alpha blend operations of bitmaps with its Alpha Blend unit; draws lines, polygons, circles using its hardware efficient & pixel accurate Bresenham line drawing Unit.

The DB9200 2D Graphics Engine provides options for higher graphics performance as a Graphics Processing Unit (GPU) with its Display List Processing Unit addition; Parallel Pixel Processing capabilities; and Memory Interface Units that unlock the graphics memory bottleneck.

DB9100 and DB9200 Family of 2D Graphics Hardware Engines

Both the DB9100 and DB9200 family supports the AMBA AXI4, AXI3, AHB; Accellera Open Core Protocol (OCP); and Altera Avalon Bus fabrics. The AXI4, AXI3, and OCP support the highest graphics memory performance. The AXI4, AXI3, AHB and OCP fabrics support ASIC & ASSP integrated circuit design teams. The AXI4 supports Altera and Xilinx FPGAs while the Avalon supports Altera FPGAs. Please start with Digital Blocks *2D Graphics Hardware Accelerator Engines* page for more information www.digitalblocks.com/ip-cores/hw-graphics-accelarator.html

Price and Availability

The DB9100 and DB9200 are available immediately in synthesizable Verilog, along with a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at http://www.digitalblocks.com

About Digital Blocks

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

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